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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/085,903	02/28/2002	Andy Wei	AMDL115\HON	4163

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EXAMINER	
LEE, HSIEN MING	
ART UNIT	PAPER NUMBER
2823	

DATE MAILED: 06/04/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/085,903	WEI ET AL.	
	Examiner	Art Unit	
	Hsien-Ming Lee	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-33* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *14-20 and 28-33* is/are allowed.

6)☒ Claim(s) *1-4,7-9,11 and 21-27* is/are rejected.

7)☒ Claim(s) *5,6,10,12 and 13* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☒ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-4, 7-9, 11 and 21-27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Suzuki et al. (US 6,423,993) in view of Osanai (US 6,380,037).

In re claims 1 and 4, Suzuki et al. in Fig.11 and related text teach the claimed method of processing, comprising:

- forming an impurity region 73 in a device region (i.e. the transistor region 77/71) of a semiconductor substrate 31/32/33, the impurity region 73 defining a junction (i.e. pn junction) and
- forming a dislocation region 39 (i.e. a plug region) in the device region, the dislocation region 39 traversing the pn junctions, i.e. with the presence of the dislocation region 39, the pn-junctions are reverse biased, resulting in suppressing current leakage in the vicinity at the end of isolation region 34 (col.11, lines 38-45); and
- forming a gate electrode 71 on the device region.

Suzuki et al. do not teach that the substrate is a semiconductor-on-insulator (SOI).

However, Suzuki et al. do suggest the applicability of the teachings to MOS solid-state image-sensing device, which usually has the SOI substrate associated with it, as evidenced by

Osanai. Osanai teaches an image sensor integrated circuit device using an SOI substrate (abstract).

Therefore, it would have been obvious to one of the ordinary skill in the art, at the time the invention was made, to apply the teachings of Suzuki et al. to a semiconductor device formed on the SOI substrate as taught by Osanai, since by doing so it would reduce power consumption, increase operation speed and avoid the influence of noise (col.1, lines 22-24, Osanai).

In re claims 2 and 3, Suzuki et al. in Fig.11 also teach the forming of the impurity region comprises forming a source/drain extension region 38 and another impurity region 73 overlapping the source/drain extension region 38, wherein the source/drain extension region 38 and the another impurity region 73 are formed by ion implantation (col. 11, lines 15-16).

In re claim **7,** Suzuki et al. in Fig.17 and related text teach the claimed method of processing, comprising:

- forming an impurity region 36 in a device region (i.e. a sensor 118 region) of a substrate 31/32/33, the impurity region 36 defining a pn-junction; and
- forming a p-type impurity region 95 in the device region 118 on both sides of a trench isolation layer 93, wherein the impurity region 95 is equivalent to the plug region 39 of Fig.11,which has dislocations associated with it and has function of traversing the pn-junctions, as stated above.

Suzuki et al. do not expressly teach forming at least two dislocation regions in the device region. However, one of the ordinary skill in the art would have been motivated to form at least two dislocation regions in the device region for a reasonable expectation of success because Suzuki et al. teach forming impurity region 95 having dislocations on both sides of the trench

isolation layer 93, which inherently suggest forming a dislocation region on each side of the trench isolation layer 93. The reason for this is that the dislocation region is formed between the isolation region and the impurity region as shown in Fig. 11,wherein a dislocation region 39 is formed between 34 and 38. Therefore, one of the ordinary skills would have been recognized that a dislocation region would between 93 and 36/38 and another dislocation region would form between 93 and 94.

In re claims 8 and 9, Suzuki et al. in Fig.17 also teach forming the impurity region comprises forming a source/drain extension region 38 (i.e. a high concentration region acts as the source/drain extension region) and another impurity region 36 overlapping the source/drain extension region 38, wherein the source/drain extension region 38 and the another impurity region 36 are formed by ion implantation.

In re claim 11, Suzuki et al. also inherently teach forming a gate electrode on the device region in light of the related text, as stated above, since the ultimate goal of Fig.17 is to form the sensor, which needs a gate electrode to perform sensor's functions.

In re claims 21 and 22, Suzuki et al. in view of Osanai also teach the claimed circuit device in light of aforementioned rejection to claims 1 and 4, comprising: a semiconductor-on-insulator substrate, as taught by Osanai, having a device region 71/77 (Suzuki et al); an impurity region 38/73 in the device region 71/77 (Suzuki et al.), the impurity region 38/73 defining a pn-junction; and a dislocation region 39 in the device region 71/77 (Suzuki et al.), the dislocation region 39 traversing the pn-junction, wherein the impurity region 38/73 comprises an extension region 38 and an overlapping region 73.

In re claims 23 and 24, Suzuki et al. in view of Osanai also teach that the dislocation region 39 traverses the pn-junction proximate the extension region 38 and the overlapping region 73, i.e. with the presence of the dislocation region 39, the pn-junctions are reverse biased, resulting in suppressing current leakage in the vicinity at the end of isolation region 34 (col.11, lines 38-45).

In re claims 25 and 27, Suzuki et al. in view of Osanai also teach comprising a gate electrode 71 (Fig.11, Suzuki et al.) and the device region comprises silicon, i.e. substrate is silicon and the electrode is composed of silicon (col.6, lines 14-15 and 60-63).

In re claim 26, Suzuki et al. also teach that the circuit device comprises a plurality of dislocation regions traversing the junction, as stated in the rejection to claim 7.

Allowable Subject Matter

3. Claims 5, 6, 10, 12, 13 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

4. Claims 14-20 and 28-33 are allowed.

5. The following is a statement of reasons for the indication of allowable subject matter: Suzuki et al. to US 6,423,993 teach all the claimed limitations, as stated above, but at least neither teach nor suggest: (1) the forming of the dislocation region comprises forming an amorphous region in the device region and heating the semiconductor-on insulator substrate to recrystallize the amorphous region (claim 5); (2) the forming of the amorphous region comprises implanting a neutral species ions into the device region (claim 6); and (3) forming a first impurity region and a second impurity region in a device region of a semiconductor-on-insulator

substrate, the first impurity region defining a first junction and the second impurity region defining a second junction; forming a first dislocation region in the device region, the first dislocation region traversing the first junction; and forming a second dislocation region in the device region, the second dislocation region traversing the second junction (claims 14 and 28).

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hsien-Ming Lee whose telephone number is 703-305-7341. The examiner can normally be reached on M-F (9:00 ~ 5:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on 703-306-2794. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7722 for regular communications and 703-308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

Hsien-Ming Lee
Examiner
Art Unit 2823

May 23, 2003